WS3233Q-20/TR

USB Type-C Port Protection Switch for CC and High-Speed Digital (SBU or D+/D-) Port

Descriptions

The WS3233Q-20/TR is a single chip USB Type-C port protection solution. The product protects CC and HSD (SBU or D+/D-) channels when stressed with voltage up to 20 V. The product also integrates IEC 61000-4-2 system level ESD protection for external pins including C_CC1, C_CC2, C_HSD1, and C_HSD2, to avoid high voltage TVS diodes near the connector. The HSD channel also supports USB2.0 signals with a high bandwidth up to 800 MHz to maintain signal integrity and eye compliance.

The WS3233Q-20/TR enables CC and HSD pins to be 20 V tolerant without interference with normal operation by providing Over-Voltage Protection (OVP) on the CC and HSD channels. If a voltage exceeds the OVP threshold on the CC and HSD lines, high voltage switches are off to isolate the rest of the system from high voltage on the connector side.

The WS3233Q-20/TR is available in a QFN3x3-20L package. Standard products are Pb-free and halogen-free.

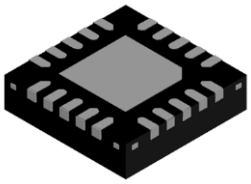
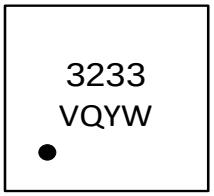


Figure 1 QFN3x3-20L (Bottom View)



3233 = Device code
VQ = Special code
Y = Year code
W = Week code

Figure 2 Marking (Top View)

Features

- Short-to-VBUS voltage up to 24 V for CC and HSD channel
- Ultra-low CC on resistance: 0.3 Ω
- Ultra-fast OVP response time: 70 ns
- HSD -3dB bandwidth: 800 MHz
- CC OVP threshold: 5.9 V
- HSD OVP threshold: 4.5 V

Applications

- Mobile handsets and tables
- Laptop PC monitors and TVs
- Docking stations

Order Information

Table 1

Device	Package	Shipping
WS3233Q-20/TR	QFN3x3-20L	3000/Reel&Tape

Pin Information

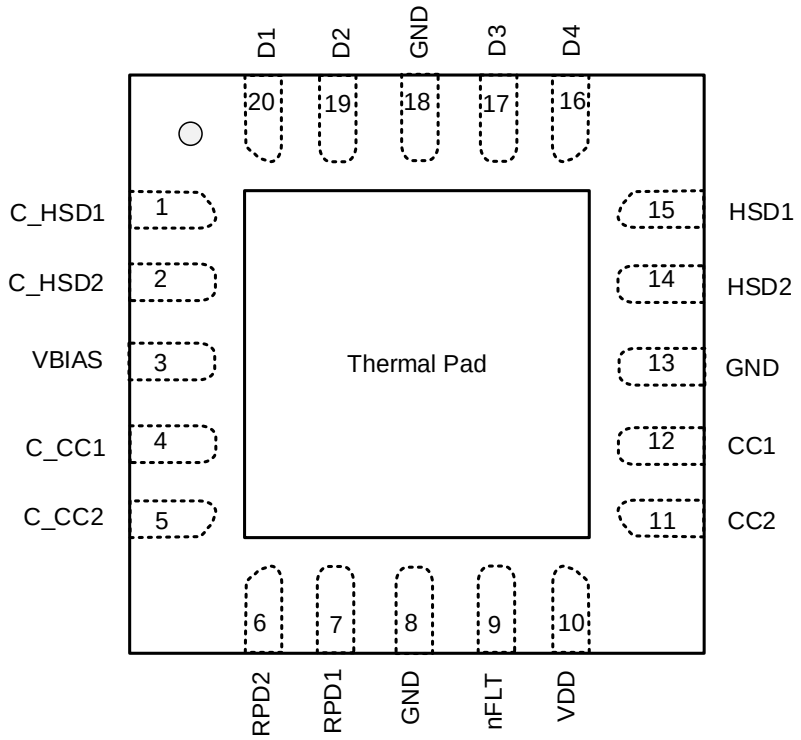


Figure 3 Pin Information (Top View)

Table 2

Pin	Function	Description
1	C_HSD1	Connector side of the HSD OVP FET. Connect to either SBU or USB2.0 pin of the USB Type-C connector.
2	C_HSD2	Connector side of the HSD OVP FET. Connect to either SBU or USB2.0 pin of the USB Type-C connector.
3	VBIAS	Pin for the ESD capacitor. Place a 0.1 µF capacitor on this pin to ground.
4	C_CC1	Connector side of the CC OVP FET. Connect to CC pin of the USB Type-C connector.
5	C_CC2	Connector side of the CC OVP FET. Connect to CC pin of the USB Type-C connector.
6	RPD2	Short to the C_CC2 if dead battery resistors are needed. Otherwise, short the pin to the GND.
7	RPD1	Short to the C_CC1 if dead battery resistors are needed. Otherwise, short the pin to the GND.
8	GND	Ground.
9	nFLT	Open drain output for fault reporting.
10	VDD	Power supply.
11	CC2	System side of the CC OVP FET. Connect to CC pin of the CC/PD controller.
12	CC1	System side of the CC OVP FET. Connect to CC pin of the CC/PD controller.
13	GND	Ground.

Pin	Function	Description
14	HSD2	System side of the HSD OVP FET. Connect to either SBU or USB2.0 pin.
15	HSD1	System side of the HSD OVP FET. Connect to either SBU or USB2.0 pin.
16	D4	IEC ESD protection pin.
17	D3	IEC ESD protection pin.
18	GND	Ground.
19	D2	IEC ESD protection pin.
20	D1	IEC ESD protection pin.
-	Thermal pad	Internally connected to the GND. Used as a heatsink. Connect to the PCB GND plane.

Block Diagram

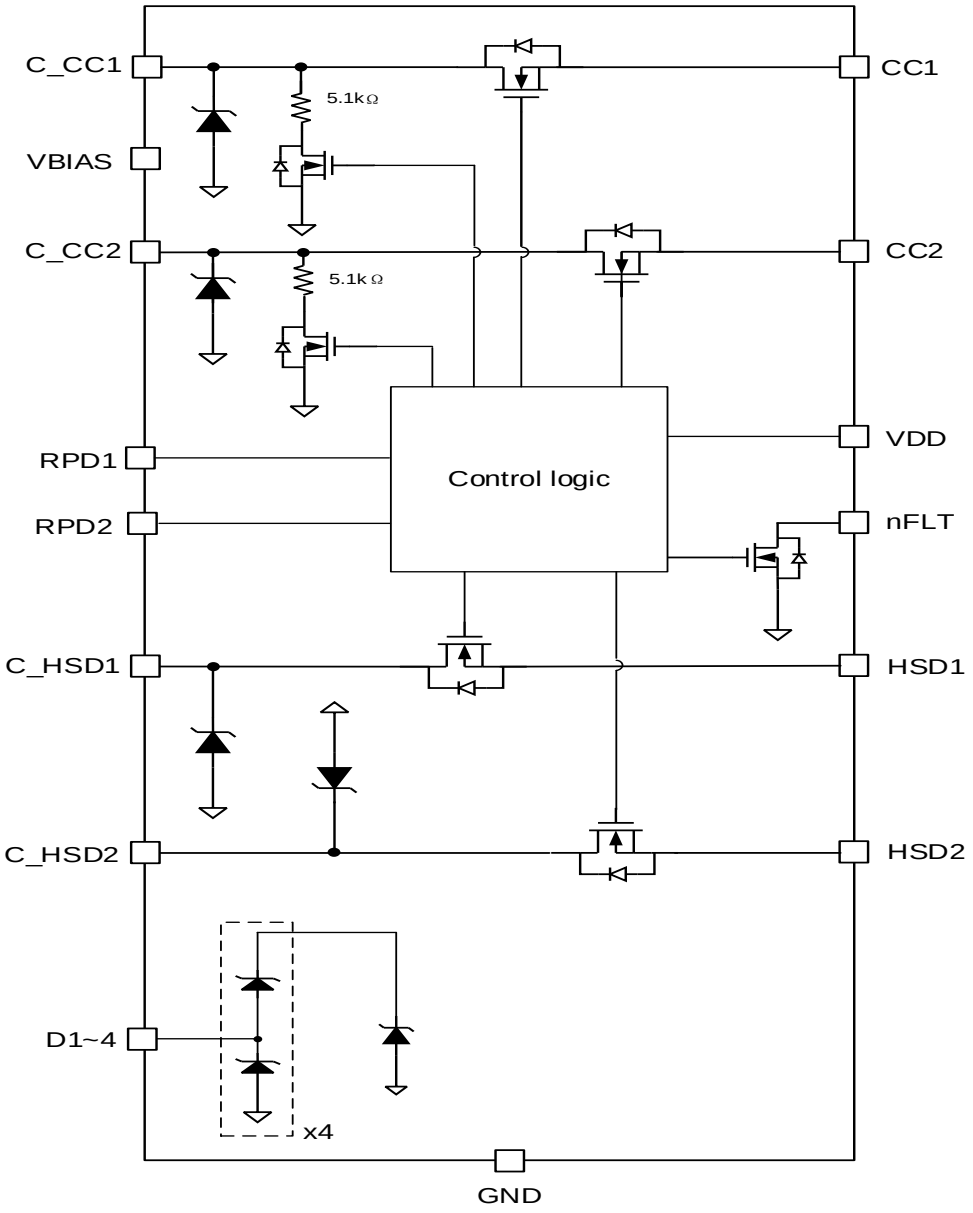


Figure 4 Block Diagram

Typical Applications

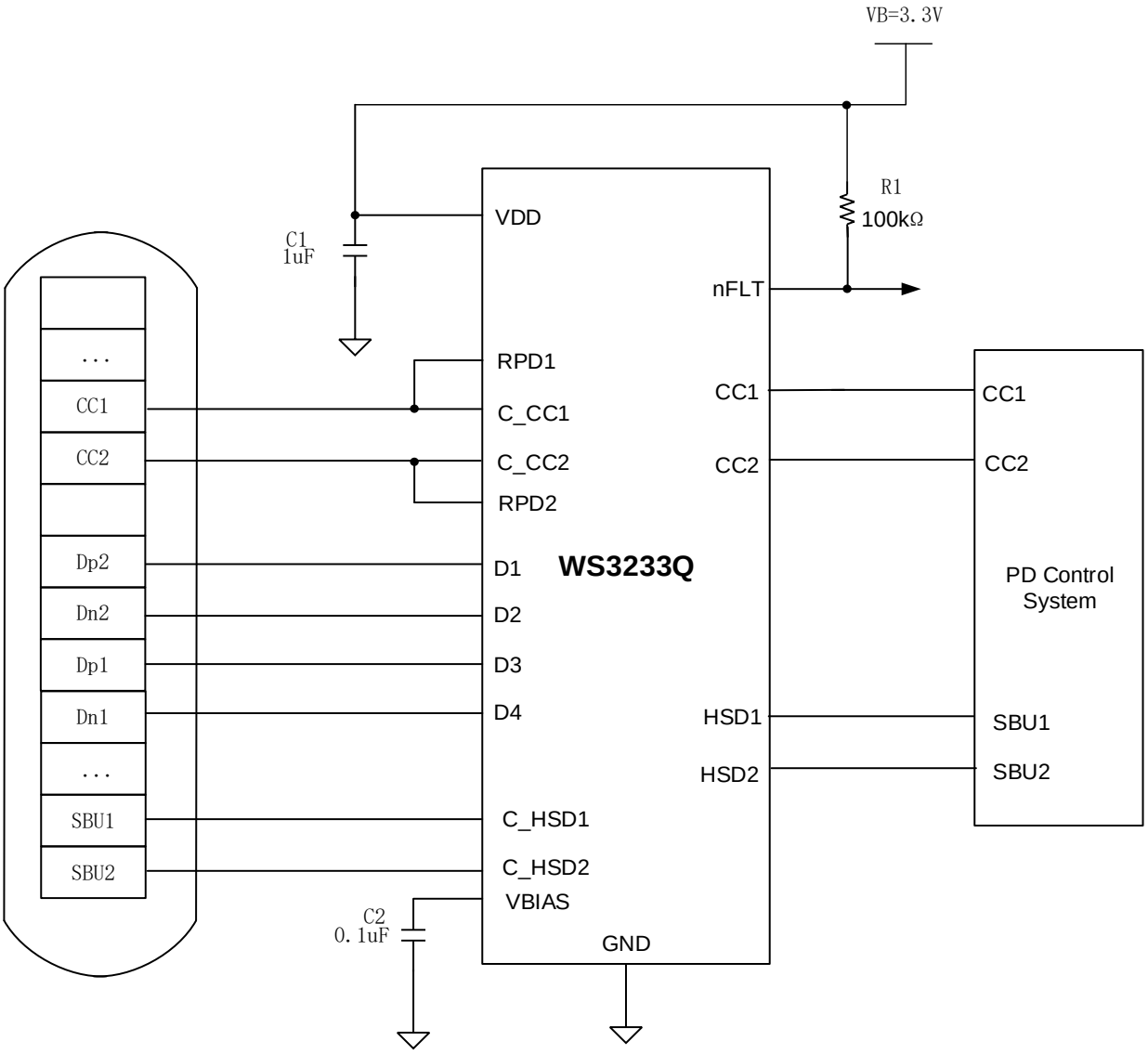


Figure 5 Typical Applications

R1 is recommended to use a 100 kΩ resistor.

C2 is recommended to be a minimum 50 V and 100 nF X7R capacitor.

Absolute Maximum Ratings

Maximum ratings are absolute ratings. Exceeding any value in table 3 might cause irreversible damage to the integrated circuit.

Table 3

Parameter	Symbol	Condition	Min.	Max.	Unit
Power	V_{VDD}	Supply voltage of VDD	-0.3	5	V
Input voltage	V_I	RPD1, RPD2	-0.3	24	V
Output voltage	V_O	nFLT	-0.3	6	V
		VBIAS	-0.3	24	V
I/O voltage	V_{IO}	CC1, CC2, HSD1, HSD2	-0.3	6	V
		C_CC1, C_CC2, C_HSD1, C_HSD2	-0.3	24	V
		D1, D2, D3, D4	-0.3	6	V
Storage temperature	T_{stg}		-65	150	˚C
Maximum junction temperature	$P_{junction}$		-	150	˚C
HBM	V_{ESD}	Human Body Model	±2000		V
CDM		Charged Device Model	±500		V
V_{C_CCx}, V_{C_HSDx} pin IEC		IEC 61000-4-2 Contact, Connector pins (V_{C_CCx}, V_{C_HSDx})	±6000		V
V_{Dx} pin IEC		IEC 61000-4-2 Contact, Connector pins (V_{Dx})	±8000		V

Recommend Operating Ratings

Table 4

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage from VDD	V_{DD}	VDD	2.7	3.3	4.5	V
Supply voltage from RPDx	V_{RPDx}	RPDx	0	-	5.5	V
CC pins in system side	V_{CCx}	CC_X	0	-	5.5	V
CC pins in connector side	V_{C_CCx}	C_CC_X	0	-	5.5	V
HSD pins in system side	V_{HSDx}	HSD_X	0	-	4.3	V
HSD pins in connector side	V_{C_HSDx}	C_HSD_X	0	-	4.3	V
I_{VCONN}	V_{CONN} Current	Current flowing into CC_X and flowing out of C_CC_X, VCC_X-VC_CC_X≤250 mV	-	-	600	mA
		Current flowing into CC_X and flowing out of C_CC_X, T_J≤105 °C	-	-	600	mA
		Current flowing into CC_X and flowing out of C_CC_X, T_J≤85 °C	-	-	1.25	A
Operating free air temperature	T_A		-40	-	85	˚C

Electrical Characteristics

Typically tested at Ta=25°C. Minimum and Maximum limits apply to the full operating ambient temperature range (-40 °C to 85 °C) unless otherwise noted.

Table 5

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply and Leakage Currents						
VDD under voltage lockout	V_{UVLO}	VDD rising from 1 V to 3 V	2.35	2.5	2.65	V
VDD UVLO hysteresis	V_{UVLO_HYS}	-	50	120	200	mV
VDD supply Current	I_{DD}	VDD=3.3 V	-	70	105	uA
$I_{C_CC_LEAK}$	Leakage current for C_CC pins when the device is powered	VDD=3.3 V, V_{C_CCx}=3.6 V, CCx floating, measure leakage into C_CCx	-	-	5	uA
$I_{C_HSD_LEAK}$	Leakage current for C_HSD pins when device is powered	VDD=3.3 V, V_{C_HSDx}=3.6 V, HSDx floating, measure leakage into C_HSDx	-	-	3	uA
$I_{C_CC_LEAK_OVP}$	Leakage current for CC pins when the device is in OVP	VDD=3.3 V, V_{C_CCx}=24 V, CCx are sets to 0 V, measure leakage into C_CCx	-	-	6	mA
$I_{C_HSD_LEAK_OVP}$	Leakage current for HSD pins when the device is in OVP	VDD=3.3 V, V_{C_HSDx}=24 V, HSDx are set to 0 V, measure leakage into C_HSDx	-	-	400	uA
$I_{CC_LEAK_OVP}$	Leakage current for CC pins when the device is in OVP	VDD=3.3 V, V_{C_CCx}=24 V, CCx are sets to 0 V, measure leakage out of CCx	-	-	1	uA
$I_{HSD_LEAK_OVP}$	Leakage current for HSD pins when the device is in OVP	VDD=3.3 V, V_{C_HSDx}=24 V, HSDx are set to 0 V, measure leakage out of HSDx	-	-	1	uA
I_{DX}	Leakage current for DX pin	V_DX=3.6 V, measure leakage into DX pins	-	-	1	uA
CC Channel						
On resistance of CC OVP FETs	R_{ON}	CCx=0 V to 5.5 V	-	300	500	mΩ
On resistance flatness	$R_{ON(FLAT)}$	Sweep CCx from 0 V to 1.2 V	-	-	10	mΩ
Equivalent on capacitance	C_{ON_CC}	Capacitance from C_CCx or CCx to GND when the device is powered. V_{C_CCx}/V_{CCx}=0 V to 1.2 V, f=400 kHz	-	40	60	pF

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Dead battery pull-down resistance	R_D	V_{C_CCx}=2.6 V	4	5.1	6	kΩ
Threshold voltage of the pull-down FET in series with R_D during dead battery	V_{TH_DB}	I_{CC}=80 uA	0.5	0.9	1.2	V
OVP threshold on C_CCx pins	V_{OVP_CC}	C_CCx rising from 5.0 V to 6.5 V	5.7	5.9	6.2	V
Hysteresis on C_CCx OVP	$V_{OVP_CC_HYS}$	-	-	130	-	mV
On bandwidth single ended (-3 dB)	BW_{ON}	R_L=50 Ω, C_L=0 pF	-	300	-	MHz
Short-to-VBUS tolerance on the C_CCx pins	$V_{ST_VBUS_CC}$	VDD=3.3 V, Hot-Plug C_CCx with 1-meter USB Type-C cable	-	-	24	V
Short-to-VBUS clamp voltage on the CCx pins	$V_{ST_VBUS_CC_CLAMP}$	VDD=3.3 V, Hot-Plug C_CCx with 1-meter USB Type-C cable; Hot-plug C_CCx=24 V	-	8	-	V
HSD Channel						
On resistance of HSD OVP FETs	R_{ON}	V_{HSDx}=0 V to 3.6 V	-	4	7	Ω
On resistance flatness	$R_{ON(FLAT)}$	-	-	-	0.7	Ω
Equivalent on capacitance	C_{ON_HSD}	Capacitance from C_HSDx or HSDx to GND when the device is powered. V_{C_HSDx}/V_{HSDx}=0.3 V to 3.6 V	-	6	-	pF
OVP threshold on C_HSDx pins	V_{OVP_HSD}	V_{C_HSDx} rising from 4.0 V to 5.5 V	4.35	4.5	4.7	V
Hysteresis on C_HSDx OVP	$V_{OVP_HSD_HYS}$	-	-	70	-	mV
On bandwidth single ended (-3 dB)	BW_{ON}	R_L=50 Ω, C_L=0 pF	-	800	-	MHz
Crosstalk	X_{TALK}	Measure crosstalk at f=1 MHz from HSD1 to C_HSD2 or HSD2 to C_HSD1.	-	-80	-	dB

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Short-to-VBUS tolerance on C_HSDx pins	$V_{ST_VBUS_HSD}$	VDD=3.3 V, Hot-Plug C_HSDx with 1-meter USB Type-C cable	-	-	24	V
Short-to-VBUS clamp voltage on HSDx pins	$V_{ST_VBUS_HSD_CLAMP}$	VDD=3.3 V, Hot-Plug C_HSDx with 1-meter USB Type-C cable; Hot-Plug V_{C_HSDx}=24 V	-	8	-	V
Dx						
Reverse stand-off voltage from Dx to GND	V_{D_G}	I_{DX} <1 μA	-	-	5.5	V
Reverse stand-off voltage from GND to Dx	V_{G_D}	-	-	-	0	V
Break-down voltage from GND to Dx	V_{BR_D}	I_{BR}=10 mA	-	0.65	-	V
Dx capacitance	C_{IO}	-	-	2.4	-	pF
nflt Pin						
Low-Level current for D_X pins	V_{OL}	I_{OL}=3 mA, Measure the voltage at nflt pin	-	-	0.4	V
Thermal Shutdown						
Thermal shutdown	T_{SD}	Enter the shutdown state	130	150	-	˚C
		Exit the shutdown state	-	110	-	˚C
Thermal hysteresis		-	-	40	-	˚C

Timing Requirements

Table 6

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power on Timings						
Time from crossing rising Power UVLO to CC and HSD OVP FETs are on	t_{ON}	VDD rising from 1 V to 3 V	-	1	3	ms
Time from crossing rising Power UVLO to CC and HSD OVP FETs are on and the dead battery resistors are turned off	t_{ON_DB}	VDD rising from 1 V to 3 V	-	4.1	8	ms
Over Voltage Protection						
OVP response time on CC pins. Time from OVP asserted to OVP FETs turn off	t_{OVP_CC}	VDD=3.3 V	-	60	-	ns

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
OVP response time on HSD pins. Time from OVP asserted to OVP FETs turn off	t_{OVP_HSD}	VDD=3.3 V	-	70	-	ns
OVP recovery time on CC pins. Once an OVP occurred, the minimum time duration until the CC FETs turn on again	$t_{OVP_DEB_CC}$	-	-	0.7	-	ms
OVP recovery time on CC pins. Once an OVP occurred, the minimum time duration until the CC FETs turn on again and the dead battery resistors turn off.	$t_{OVP_DEB_CC_DB}$	-	-	4.6	-	ms
OVP recovery time on HSD pins. Once an OVP occurred, the minimum time duration until the HSD FETs turn on again	$t_{OVP_DEB_HSD}$	-	-	0.6	-	ms
OVP response time on CC pins. Time from OVP removal to the CC FETs turn on again, if the device has been in OVP > 0.6 ms	$t_{OVP_RE_CC}$	-	-	0.4	-	ms
OVP response time on CC pins. An OVP occurred, the minimum time duration until the CC FETs turn on again and the dead battery resistors turn off, if the device has been in OVP > 0.6 ms	$t_{OVP_RE_CC_DB}$	-	-	4.35	-	ms
OVP response time on HSD pins. Time from OVP removal to the HSD FETs turn back on, if the device has been in OVP > 0.6 ms	$t_{OVP_RE_HSD}$	-	-	0.3	-	ms
Time from OVP asserted to nFTL assertion	$t_{OVP_nFTL_TRIG}$	-	-	20	-	us
Time from OVP FETs turn on after an OVP to nFTL de-assertion	$t_{OVP_nFTL_RELEASE}$	-	-	4.1	-	ms

Working State Modes

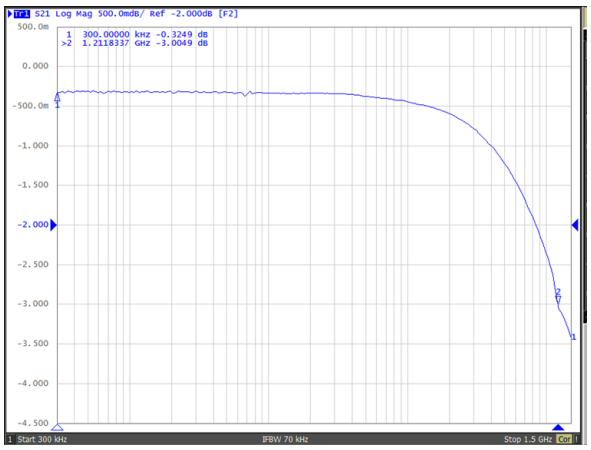
The WS3233Q-20/TR working state is shown in Table 7 below. The "X" in the table means the value does not matter.

Table 7

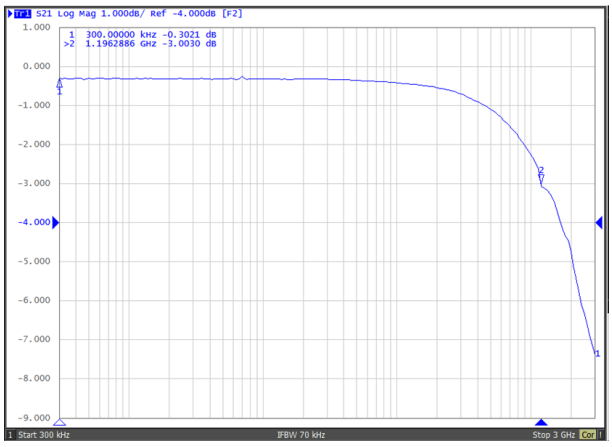
Input					Output		
VDD	**C_CCx**	**C_HSDx**	**RPDx**	**TJ**	**nFLT**	**CCx**	**HSDx**
<UVLO	X	X	CCx	X	High-Z	OFF	OFF
	X	X	GND	X	High-Z	OFF	OFF
>UVLO	<OVP	<OVP	CCx	<TSD	High-Z	ON	ON
	>OVP	X	CCx	<TSD	Low	OFF	OFF
	X	>OVP	CCx	<TSD	Low	OFF	OFF
	System ESD trigger OVP	X	X	<TSD	Low	OFF	OFF
	X	X	CCx	>TSD	Low	OFF	OFF
	<OVP	<OVP	GND	<TSD	High-Z	ON	ON
	>OVP	X	GND	<TSD	Low	OFF	OFF
	X	>OVP	GND	<TSD	Low	OFF	OFF
	X	X	GND	>TSD	Low	OFF	OFF

Typical Characteristics

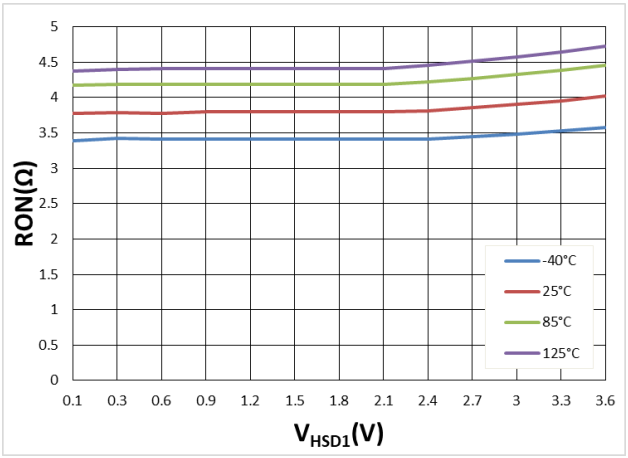
Typically tested at Ta=25˚C, unless otherwise noted.



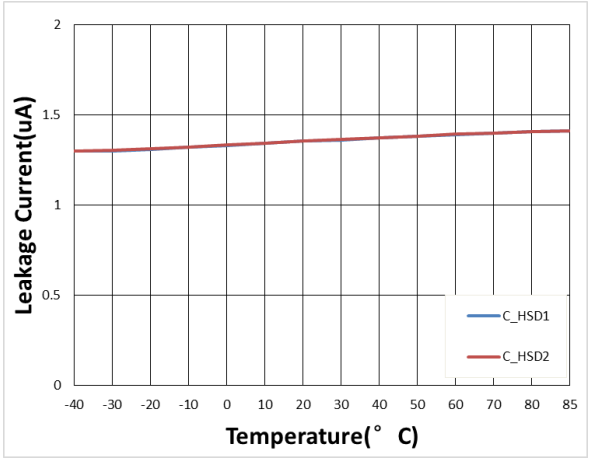
HSD1 BW



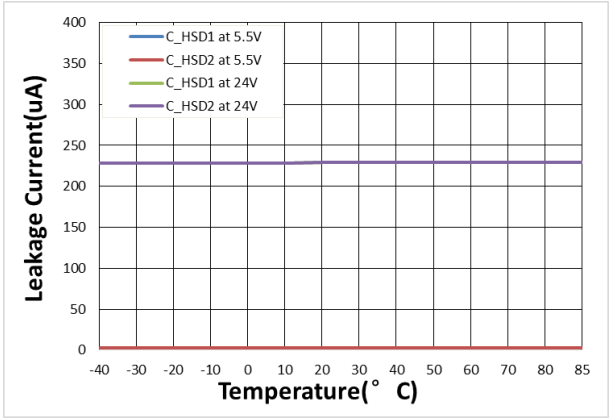
HSD2 BW



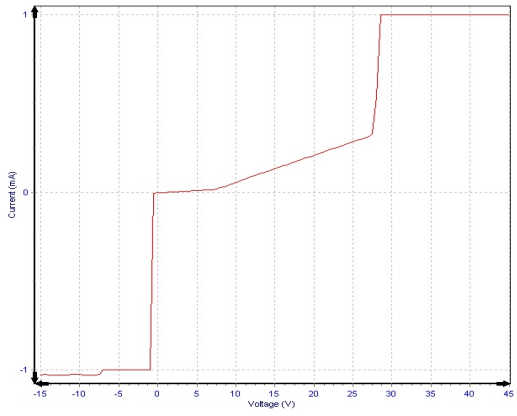
HSD R_{ON} Flatness



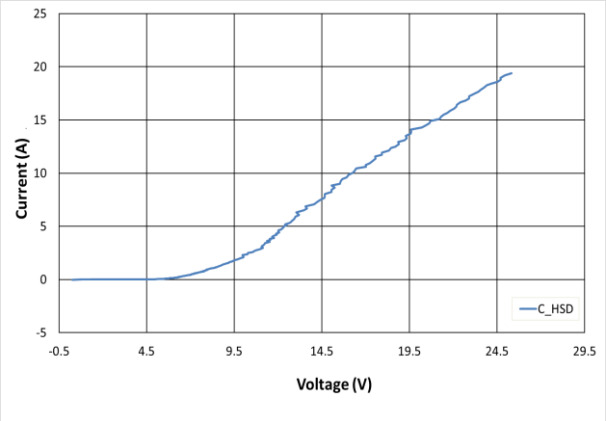
HSD Path Leakage Current vs Ambient Temperature at 3.6 V



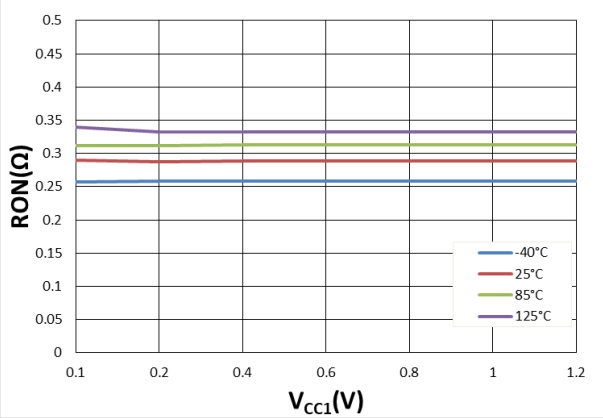
C_HSD OVP Leakage Current vs Ambient Temperature at 5.5 V and 24 V



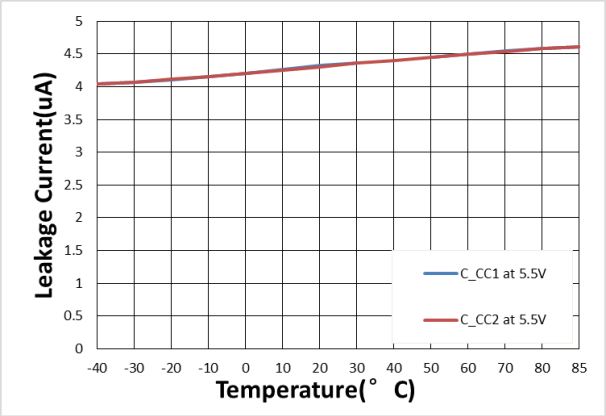
C_HSD IV Curve



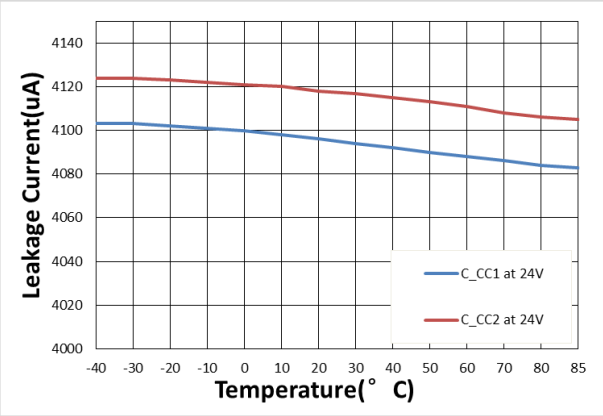
C_HSD TLP Curve Unpowered



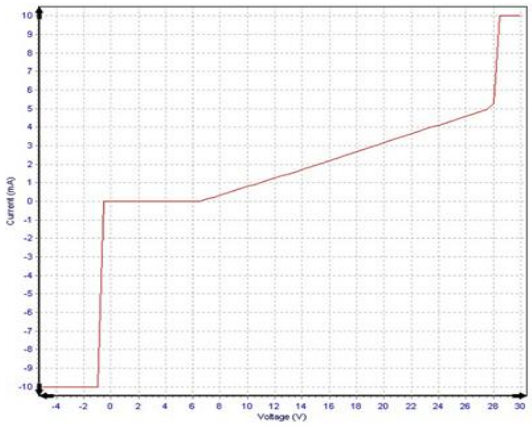
CC R_{ON} Flatness



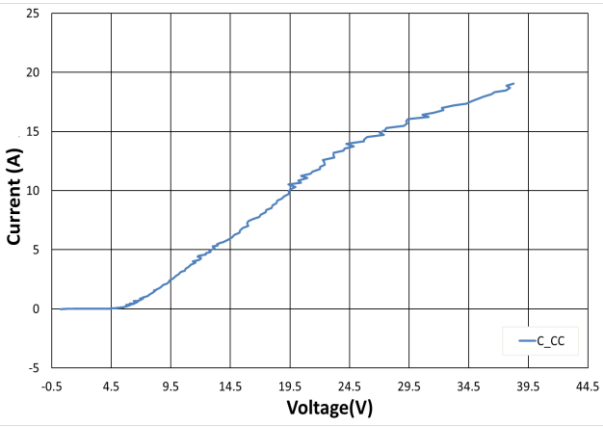
C_CC Path Leakage Current vs Ambient Temperature at C_CC=5.5 V



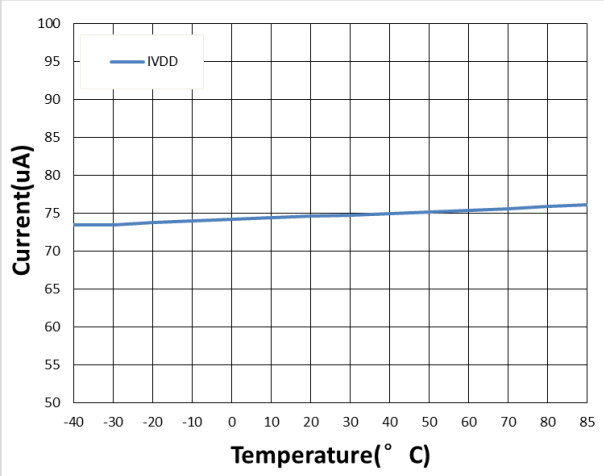
C_CC OVP Leakage Current vs Ambient Temperature at C_CC=24 V



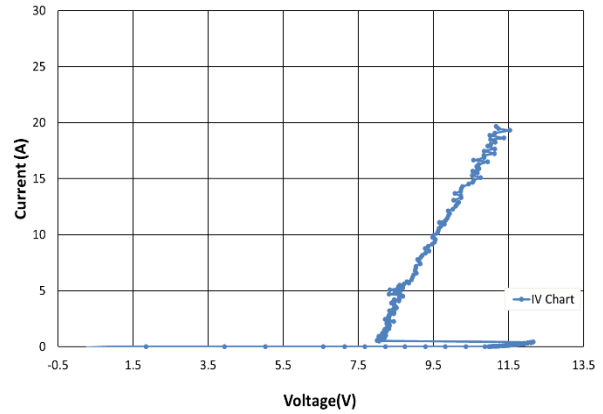
C_CC IV Curve



C_CC TLP Curve Unpowered



VDD Supply Leakage vs Ambient Temperature at 3.6 V



D_X TLP Curve

Operation Information

Function Description

The WS3233Q-20/TR integrates high voltage MOSFETs, fast over voltage comparators, and high voltage ESD blocks. The device prevents USB devices from being damaged in extreme scenarios such as VBUS shorts to CC or HSD. The CC pin has a low R_{ON} MOSFET to support a typical 0.6 A capacity for Type-C ports Vconn applications. HSD channel with 850 MHz -3 dB bandwidth keeps high quality signal transmission.

Under Voltage Lockout

The Under Voltage Lockout (UVLO) comparator monitors the VDD voltage to configure chip functions. If VDD is higher than UVLO threshold, the device enables the CC OVP function and turns off the RPD. If VDD is lower than UVLO, the device enters the dead battery mode if the RPD is pulled to the CC pin.

nFLT

The nFLT pin is an open drain output indicating fault events. The nFLT pin becomes low if CCx, HSDx over-voltage and/or TSD event happen. After fault events disappear, the nFLT recovers to high state automatically. If VDD is lower than UVLO, the nFLT keeps the High-Z state.

Over Temperature Protection

The WS3233Q-20/TR also provides the Over Temperature Protection (OTP). Once IC temperature is above the threshold, the device disconnects OVP MOSFETs, enters the dead battery mode and re-starts until junction temperature falls below its hysteresis.

Over Voltage Protection

The WS3233Q-20/TR integrates a high accuracy and ultra-fast OVP block to prevent USB devices from damage in extreme conditions such as VBUS shorts to CC. A high accuracy OVP monitors CCx and HSDx pins voltage all the time. If input voltage is higher than the threshold, the switch turns off after the response time. To avoid Type-C disconnection in ESD events, the RPD presents on the CC pin to keep connected after the OVP is triggered.

Dead-battery Mode

To use a USB PD adapter to supply power for the VBUS, the RD must be exposed on CC pins. However, when an OVP MOSFET is used to protect the USB Type-C port between the connector and CC of internal control block and power supply voltage is lower than UVLO, it blocks the RD resistor of the controller. The WS3233Q-20/TR integrates the dead-battery RD to keep Type-C connection instead when the RPD is enabled.

VBIAS

The WS3233Q-20/TR integrates a forward biased diode from the VBIAS pin to the CCx and HSDx pins to deal with IEC 61000-4-2 ESD strikes. Considering the short-to-VBUS event at 20 V and the occurrence of the around 2 times high voltage ringing spike, a 50-V 100-nF X7R capacitor is recommended to use near the VBIAS pin.

Application Information

PCB Layout Guide

For best performance, the power supply capacitor needs to be placed close to the device and the ESD protection capacitor needs to be placed close to the VBIAS pin. The capacitor needs to be attached to a solid ground to minimize effects from voltage disturbances. The USB2.0 and SBU lines need to be routed as short as possible. The device needs to be placed near the Type-C connector.

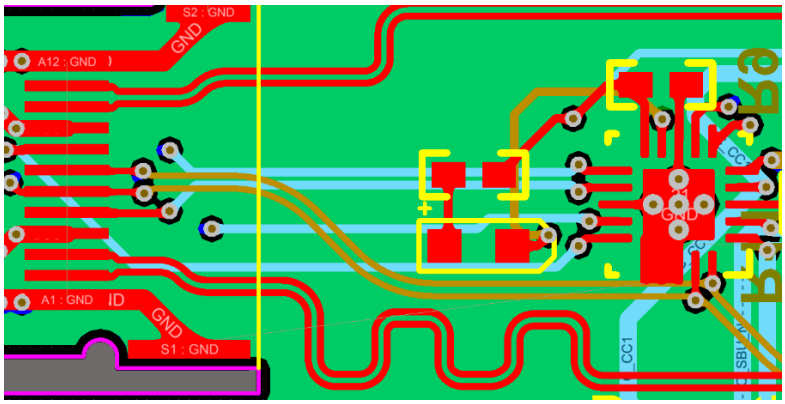
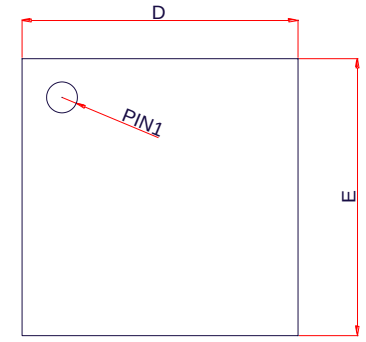


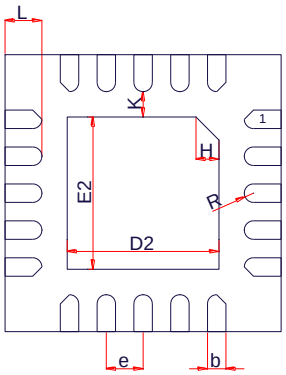
Figure 6 Layout Example (Top of the PCB)

Package Outline Dimensions

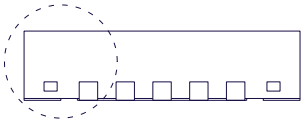
QFN3x3-20L



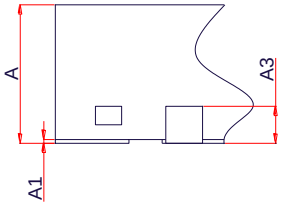
Top View

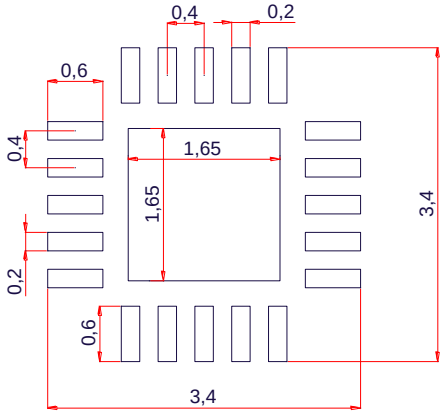


Bottom View



Side View

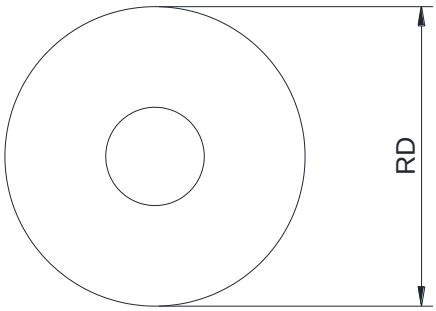




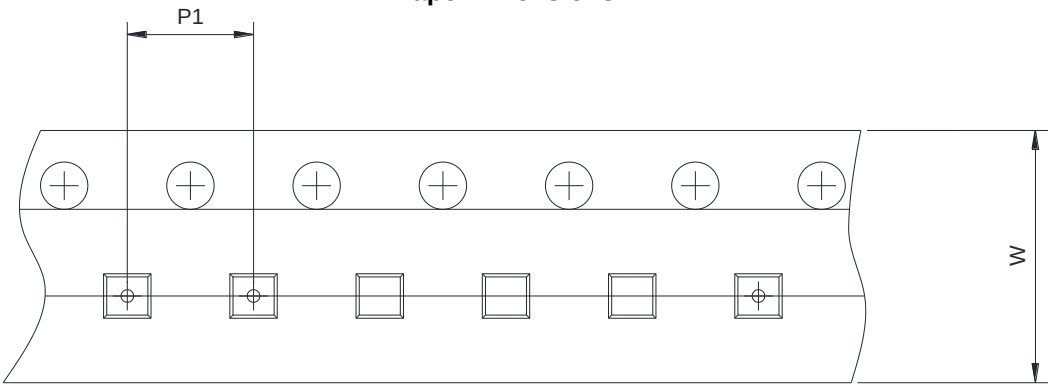
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 Ref	
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.55	1.65	1.75
E2	1.55	1.65	1.75
e		0.40 BSC	
H		0.25 REF	
K		0.275 REF	
L	0.35	0.40	0.45
R	0.075	-	-

Tape and Reel Information

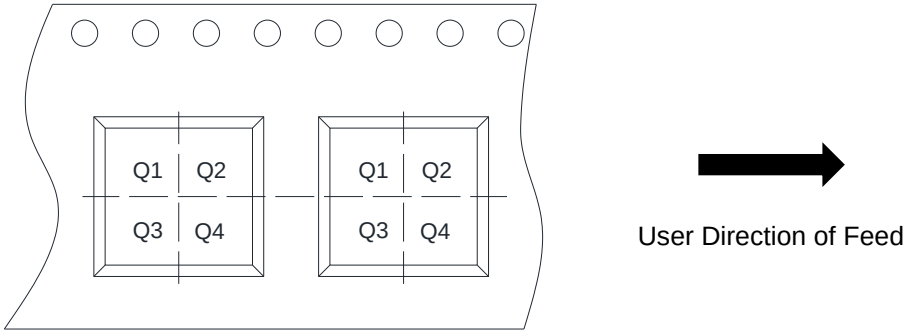
Reel Dimensions



Tape Dimensions



Quadrant Assignments for PIN1 Orientation in Tape



RD	Reel dimension	☐ 7inch ☑ 13inch
W	Overall width of the carrier tape	☐ 8mm ☑ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm ☐ 4mm ☑ 8mm
Pin1	Pin1 quadrant	☐ Q1 ☑ Q2 ☐ Q3 ☐ Q4